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# VLSI 實驗

## Lab1

### Environment setup

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在個人資料夾按右鍵 → 開啟終端機

1. 進到Data\_in\_teacher資料夾  
指令"`cd Data_in_teacher`"
2. 查看Data in teacher裡面有無cic18資料夾  
指令"`ls`"
3. 創立自己學號資料夾，並複製cic18資料夾，  
到學號資料夾下。

指令"`mkdir ~/學號`"

指令"`cp -r cic18~/學號/`"

4. 輸入"`source ~/work.cshrc`"
5. 選a，按Enter
6. 進入cic18資料夾

輸入"`cd ~/學號/cic18`"

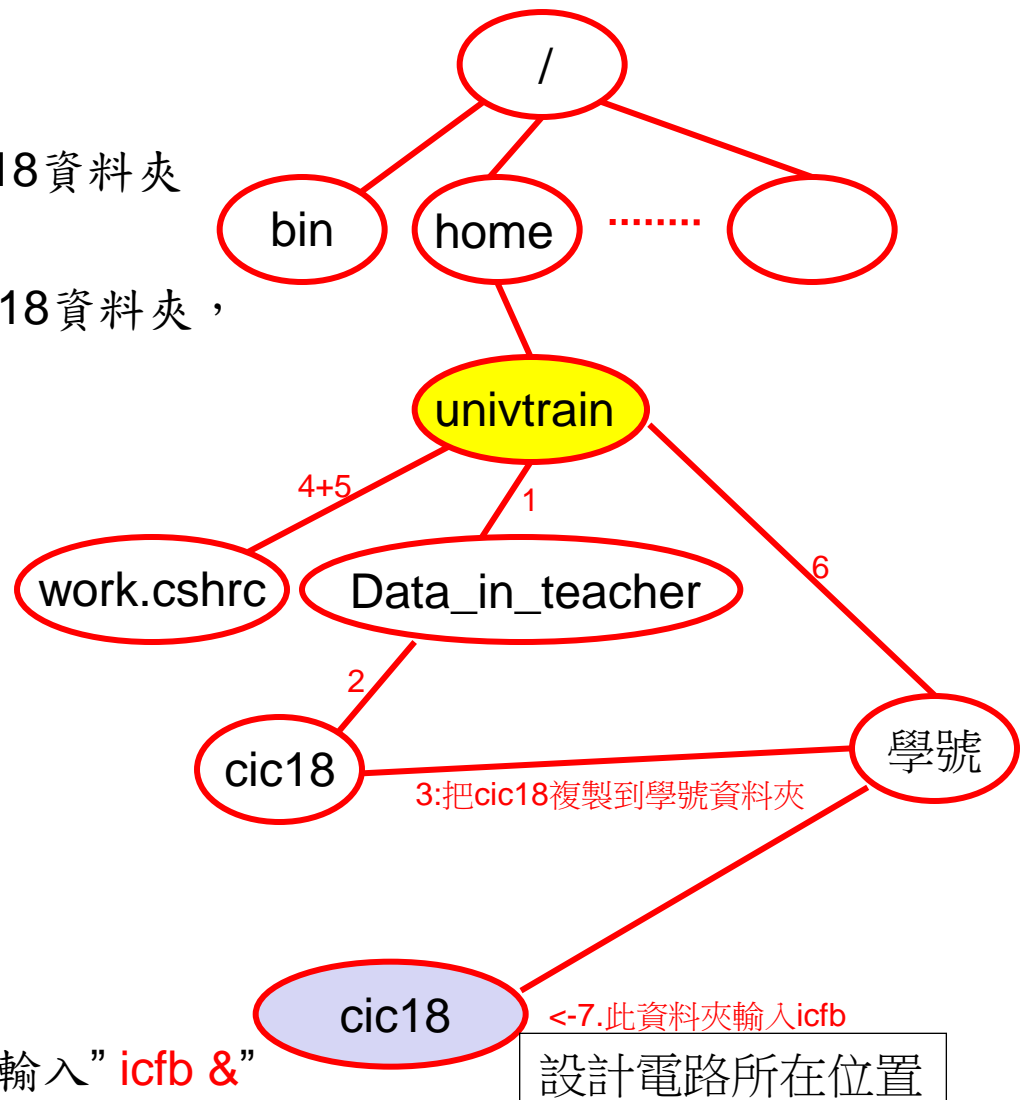
7. 輸入"`icfb &`"

p.s. 以後登入後只需要

1. 輸入"`source work.cshrc`"(選a)

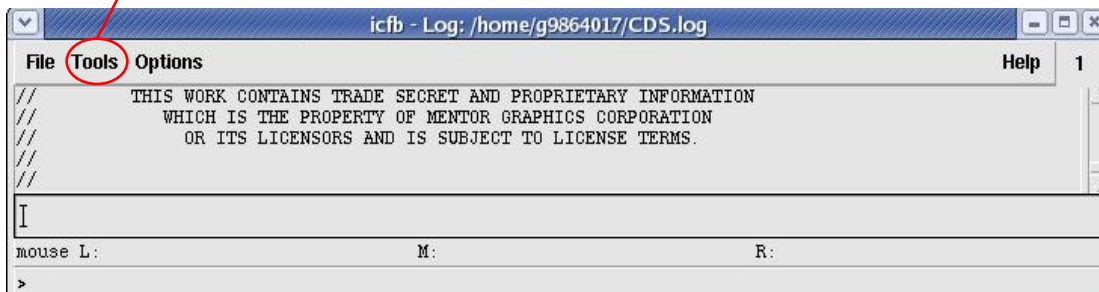
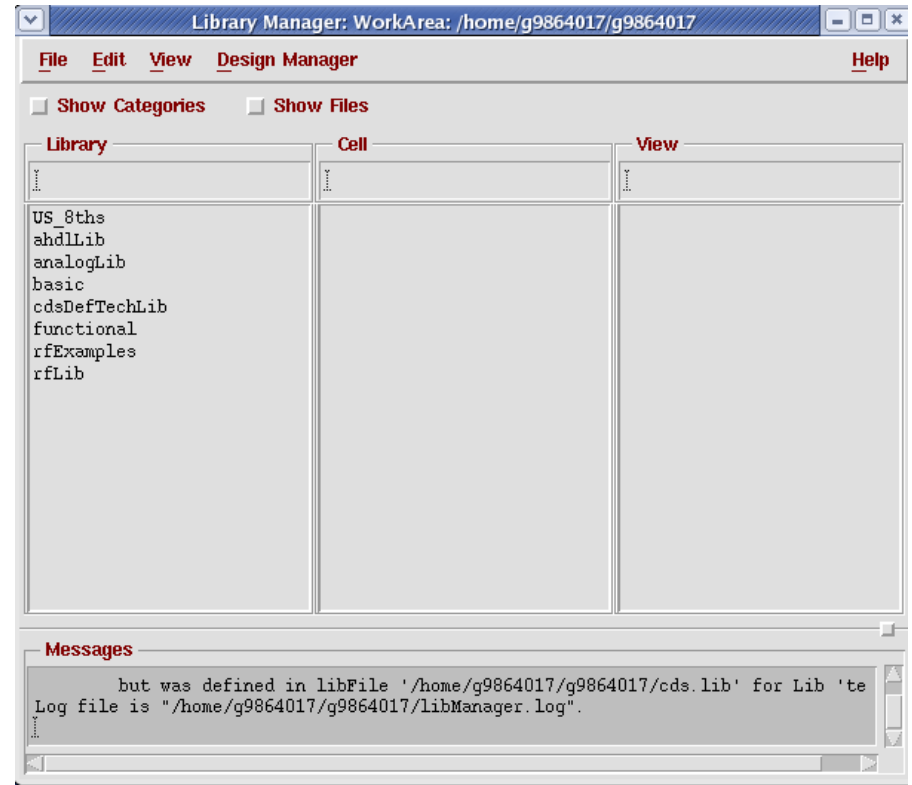
2. 輸入"`cd /學號/cic18`"

3. 輸入"`icfb &`"



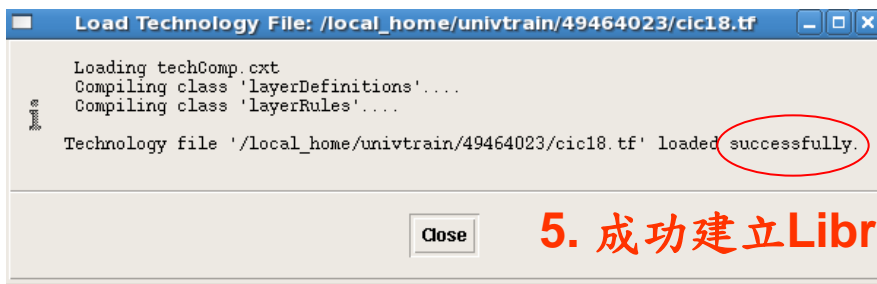
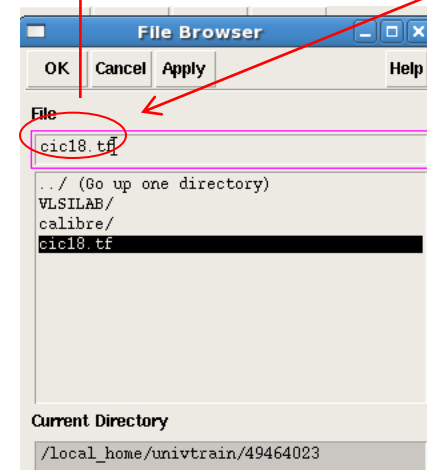
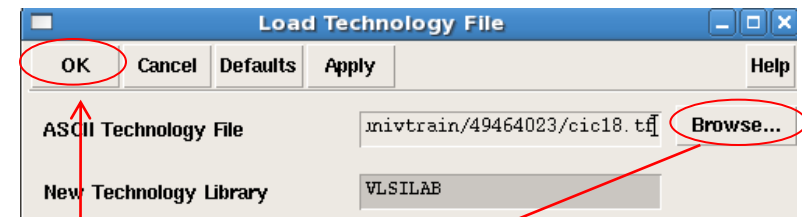
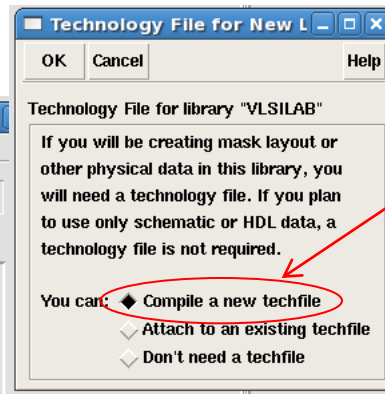
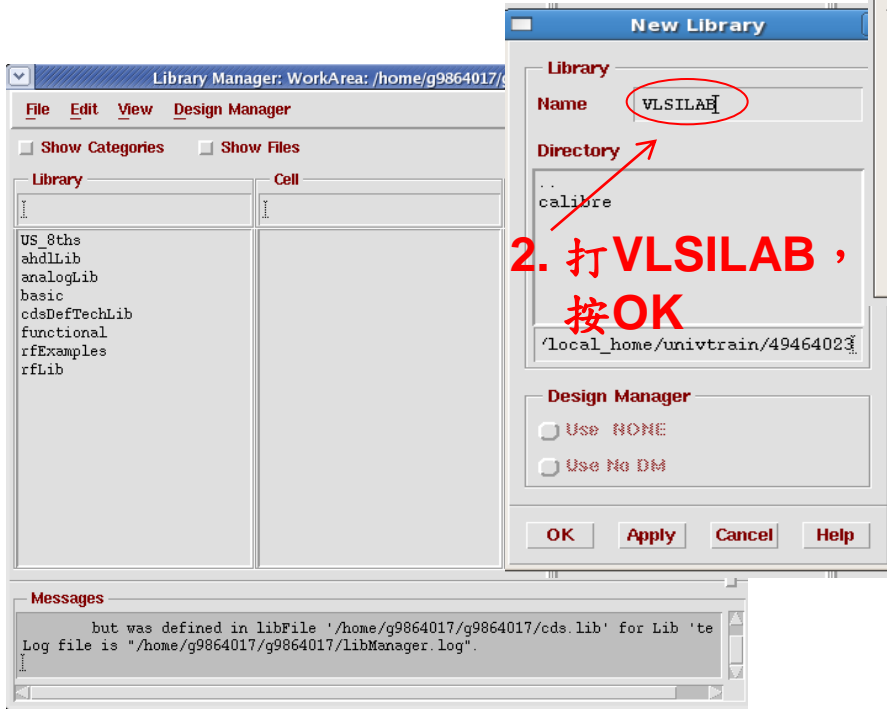
# 建Library(1/2)

- Tools → Library Manager...



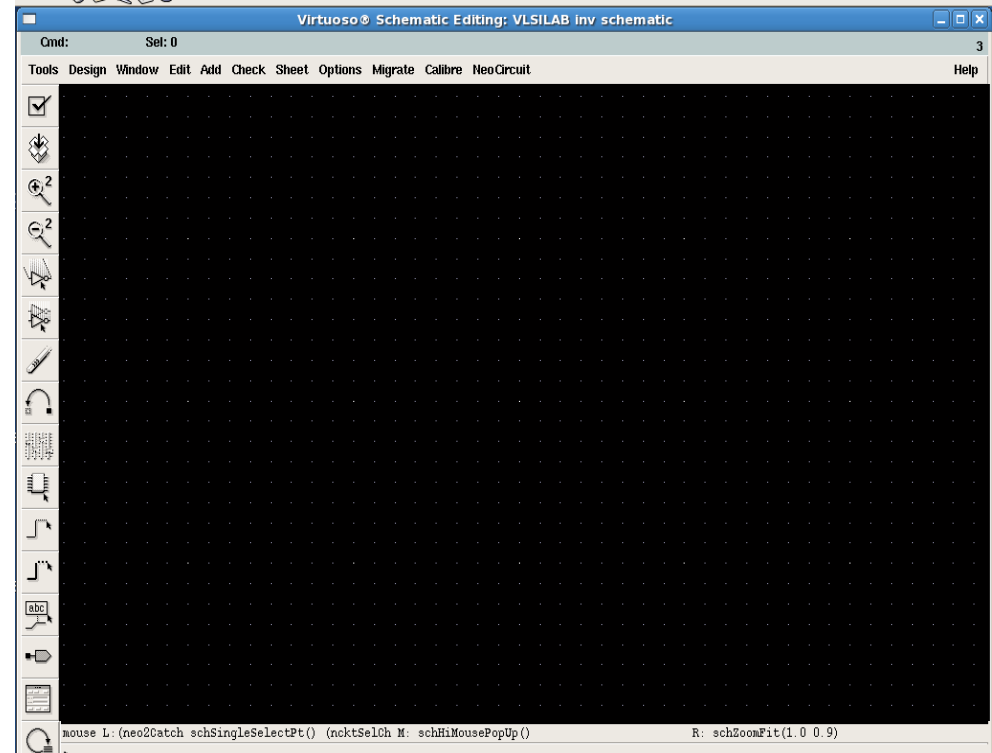
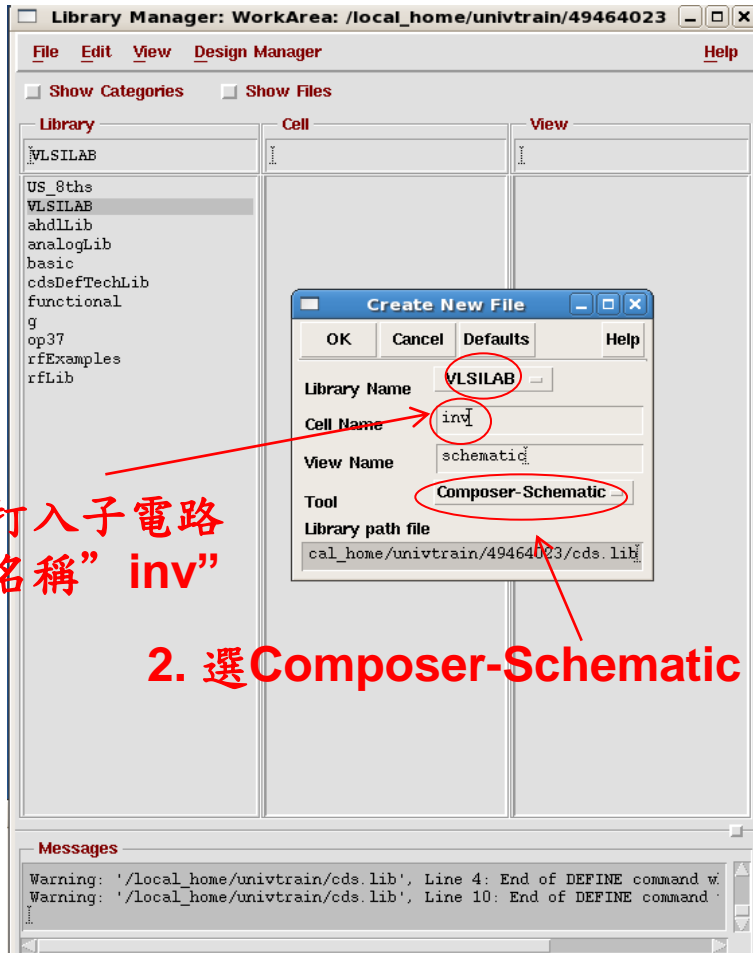
# 建Library(2/2)

1. 點選File → New → Library...



















# 新增Schematic(1/4)

1. 點選VLSILAB，接著再點選File → New → Cell View...



## 新增Schematic(2/4)

### ● 指令Icon

	儲存(快速鍵：Shift+s)		屬性(快速鍵：q)
	放大2倍(快速鍵：])		Pin(快速鍵：p)
	縮小2倍(快速鍵：[)		Line
	擴展(快速鍵：m)		Rectangle
	Copy(快速鍵：c)		Label(快速鍵：l)
	移動(快速鍵：m)		Selection Box
	刪除(快速鍵：del鍵)		Cmd option
	Undo(快速鍵：u)		Repeat(快速鍵：Shift+u)

# 新增Schematic(3/4)

## 1. 增加元件，按熱鍵 “i”

2. 按Browse選取元件

3. 選取analogLib→nmos4→symbol

4. 設定電晶體的長、寬

5. 點一下即可出現nmos4

Library	Category	Cell	View
analogLib	Actives	nmos4	symbol

# 新增Schematic(4/4)

The image shows a screenshot of the Virtuoso Schematic Editor interface. The main window displays a schematic of a CMOS inverter. The input is labeled **Vin** and the output is labeled **Vout**. The circuit consists of two transistors: an NMOS transistor (M0) with parameters  $I=350.00n$  and  $w=3u$ , and a PMOS transistor (M1) with parameters  $I=350.00n$  and  $w=9u$ . The PMOS gate is connected to the output **Vout**, and the NMOS gate is connected to the input **Vin**. The PMOS source is connected to **vdd** and the NMOS source is connected to **gnd**. The gates are connected to each other.

Annotations in red text include:

- 記得檢查和存檔** (Remember to check and save) pointing to the save icon in the toolbar.
- 連接線，熱鍵 "w"** (Connections, hotkey "w") pointing to the connection lines between the transistors.
- Pin腳，熱鍵 "p"** (Pin foot, hotkey "p") pointing to the input and output pins.

An **Add Pin** dialog box is open in the bottom right corner. The **Pin Names** field contains **Vin**. The **Direction** is set to **input**. The **Usage** is set to **schematic**. The **Attach Net Expression** is set to **No**. The **Property Name** and **Default Net Name** fields are empty. The **Font Height** is set to **0.0625** and the **Font Style** is set to **stick**. The **Rotate**, **Sideways**, **Upside Down**, and **Show Sensitivity >>** buttons are visible at the bottom of the dialog.

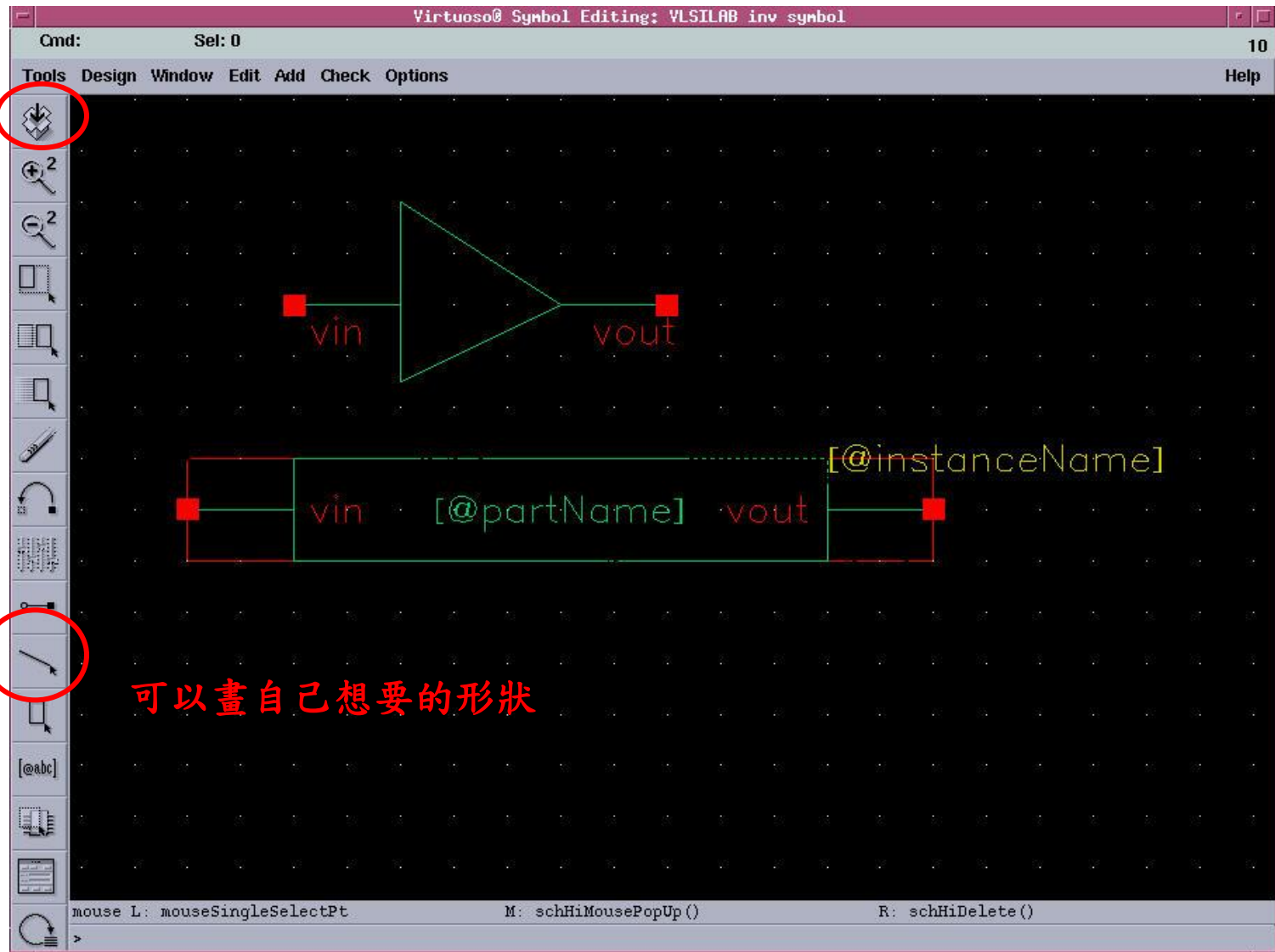


# 建立symbol(1/2)

## 1. Design → Create Cellview → From Cellview

The screenshot shows the Virtuoso Schematic Editing interface. The menu path is: Design → Create Cellview → From Cellview... (indicated by red circles). An orange arrow labeled 'Vin' points to the 'Cellview From Cellview' dialog box. The 'Cellview From Cellview' dialog has the following fields: Library Name (VLSILAB), Cell Name (inv), and From View Name. The 'Symbol Generation Options' dialog has the following fields: Library Name (VLSILAB), Cell Name (inv), View Name (symbol), and Pin Specifications (Left Pins: vin, Right Pins: vout, Top Pins, Bottom Pins). The 'Symbol Generation Options' dialog also has checkboxes for Load/Save, Edit Attributes, Edit Labels, and Edit Properties.

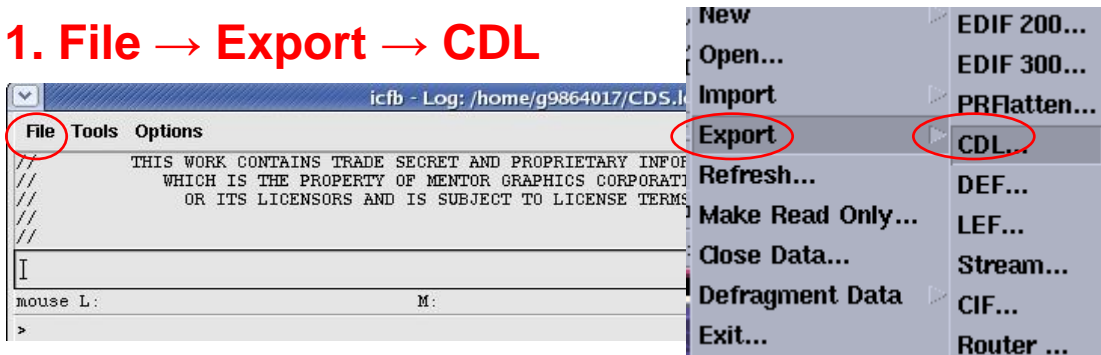
# 建立symbol(2/2)



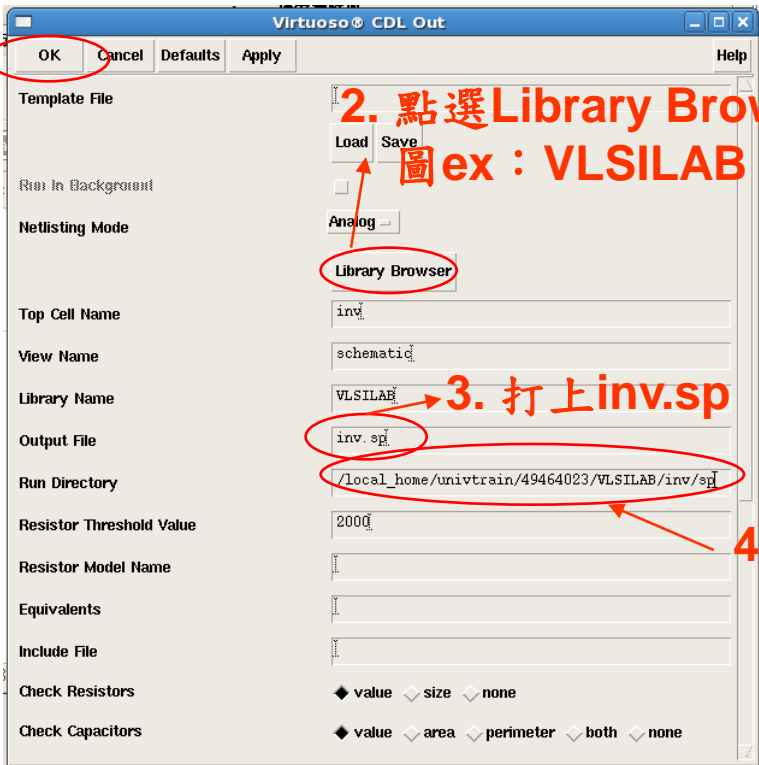
可以畫自己想要的形狀

# 轉SP檔(1/2)

## 1. File → Export → CDL



5.



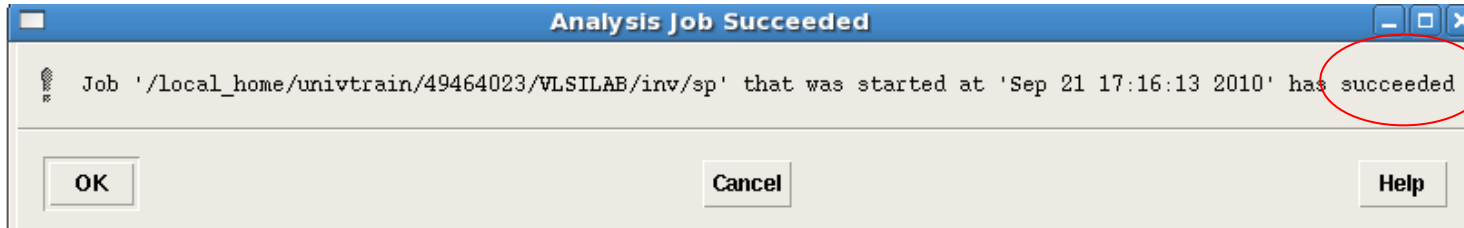
2. 點選Library Browser，選擇要輸出sp檔的電路  
圖ex：VLSILAB → inv → schematic

3. 打上inv.sp

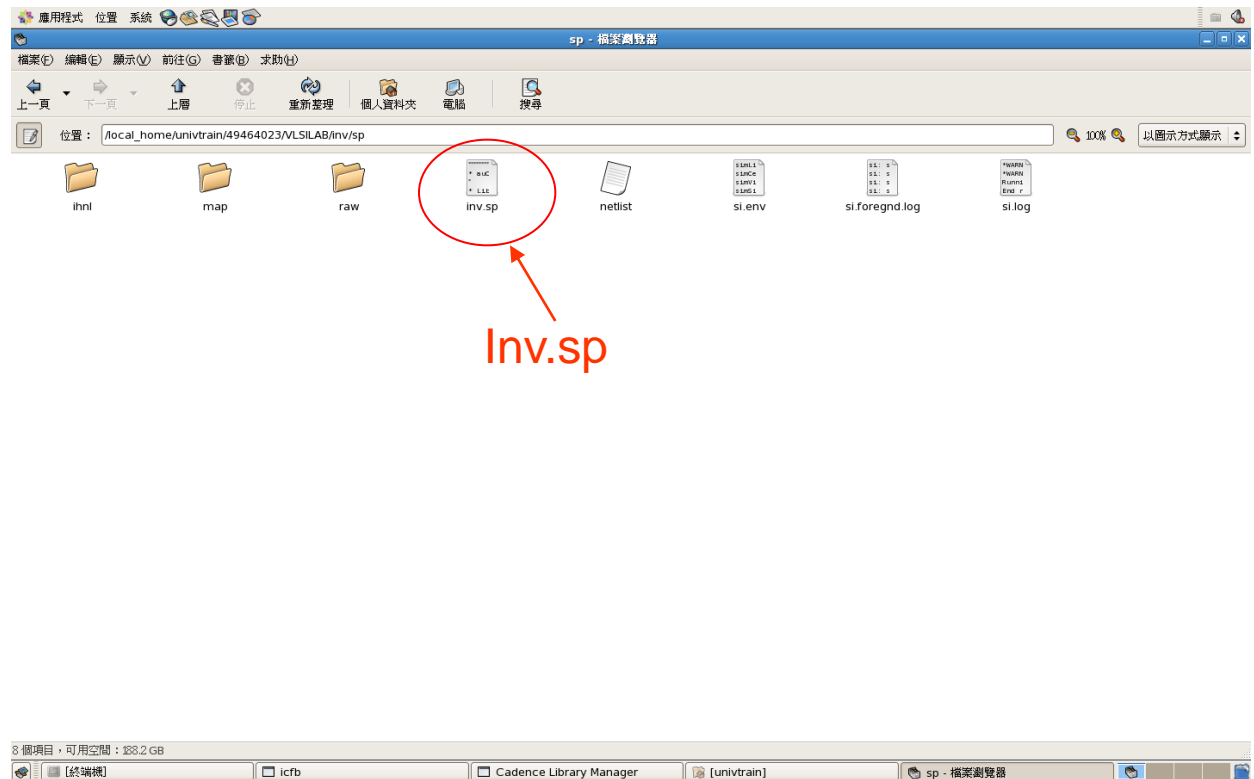
4. sp檔存放路徑



# 轉SP檔(2/2)



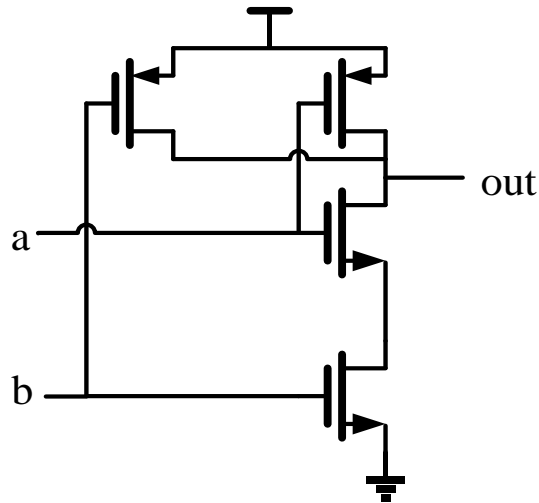
轉檔成功



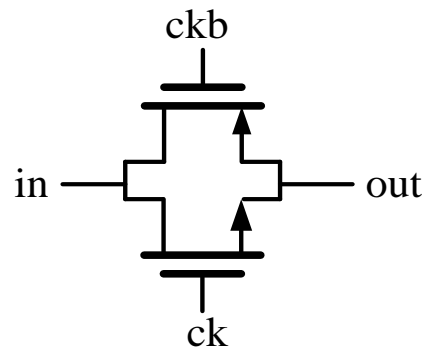
Inv.sp

# Assignment

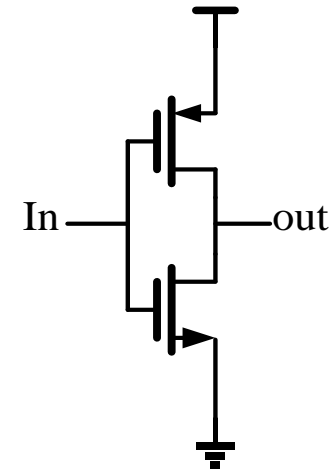
- 畫出NAND2、Transmission gate、inverter
- 建立symbol
- 轉出sp檔



NAND2



Transmission gate



inverter

PMOS (W/L)=0.75um/0.18um NMOS (W/L)=0.25um/0.18um